**Practice Questions**

1. Find the 1’s and 2’s complements of the following 8-digit binary numbers: 10101110; 10000001; 10000000; 00000001; and 00000000.
2. Draw the basic VLSI design flow and briefly explain the design flow.
3. Write the differences between analog and digital signals.
4. Represent decimal number 3624 in (a) BCD (b) Gray code, and (c) as a binary number.
5. What is Moore’s law? What are the three major design specifications for an IC chip?
6. Perform the arithmetic operations (+52) + (— 23), (—52) — (—23) and (—52) + (—23) in binary using the 2’s complement representation for negative numbers. You may choose an appropriate length for the bit sequence for the purpose in each case.
7. How many approaches are there in VLSI design? What do you think, which one is better?
8. Reduce the following Boolean expressions :
9. ABC + A'B'C + A'BC + ABC' + A'B'C'
10. BC + AC' + AB + BCD
11. [(CD)' + A' ]' + A + CD + AB
12. (A + C + D)(A + C + D)(A + C + D' )(A + C' + D)(A + B' )
13. Implement XOR and XNOR gates using: NOR gates only and NAND gates only.
14. Write the differences between Verilog and C programming.
15. Express the following functions both as a sum of minterms and a product of maxterms
16. F(A, B, C, D) = D(A' + B) + B'D
17. F(w, x, y, z) = y'z + wxy' + wxz' + w'x'z
18. F(A, B, C) = (A' + B)(B' + C)
19. F(x, y, z) = (xy + z)(y + xz)
20. Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC.
21. Write a short note on - Operators used in Verilog.
22. With the help of an example, explain conditional operator used in Verilog
23. Write the following operator from highest to lowest according to their precedence - logical, Arithmetic,  Relational, conditional,  bitwise.
24. In Verilog, how many levels of abstractions are there? Name them.
25. Implement a Full adder in an active low 3:8 decoder.
26. Design a Full adder using two half adders. Write the HDL code for a full adder circuit in gate-level technique along with the testbench code.
27. XOR and XNOR gates can be used as a buffer as well as an inverter’, Justify.
28. Design and explain the operation of a 3 bit Adder Subtractor Block using FAs and XNOR gates only
29. Obtain the minimized expression for the following 4-varible Boolean expression using K-map method and implement the minimized expression using NAND gates only.

F(P,Q,R,S) = П M (0,1,4,10,11,14).d(2,7,8,13)

1. Obtain the minimized expression for the following 4 variable Boolean expression using K-map method and implement the minimized expression using NOR gates only

F(A,B,C,D)= ∑m(0,2,5,10,11,15) + d(1,3,7)